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Attorney Docket No. 95-553-US

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION

(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

Charge any shortfall to Dep. Acct. 12-1445.

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (2) is being provided in addition to:

- (1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.


Copies of these references may be found in the file of commonly-owned, copending U.S. Patent Application No. 08/340,144 and, although NOT provided herewith, will be supplied upon request of the examiner.

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This INFORMATION DISCLOSURE CITATION corresponds to an information disclosure citation filed in commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of the references cited herein can be found in the file of that application, but will be supplied upon request of the examiner.

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

It would appear that the most relevant ones of the references cited herein are those having the term "probe" or "test" in their title. For example, the following (from the lists at page 3, et seq., below):

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MANUFACTURING METHOD FOR AN ELECTRONIC COMPONENT		
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<u>4,647,959</u>	<u>Smith; 3/87</u>	<u>357/74</u>
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<u>4,641,426</u>	<u>Hartman, et al.; 2/87</u>	<u>29/839</u>
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<u>4,615,573</u>	<u>White, et al.; 10/86</u>	<u>339/17M</u>
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<u>4,597,617</u>	<u>Enochs; 7/86</u>	<u>339/17 CF</u>
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<u>4,532,152</u>	<u>Elarde; 7/85</u>	<u>427/96</u>
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<u>4,442,967</u>	<u>van de Pas, et al.; 4/84</u>	<u>228/159</u>
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<u>4,422,568</u>	<u>Elles, et al.; 12/83</u>	<u>228/111</u>
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<u>4,419,818</u>	<u>Grabbe; 12/83</u>	<u>29/832</u>
METHOD FOR MANUFACTURING SUBSTRATE WITH SELECTIVELY TRIMMABLE RESISTORS BETWEEN SIGNAL LEADS AND GROUND STRUCTURE		
<u>4,417,392</u>	<u>Ibrahim, et al.; 11/83</u>	<u>29/840</u>
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ELECTRICAL CIRCUIT BOARD WIRING		
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ELECTRICAL INDUCTOR AND METHOD OF MAKING THE SAME		
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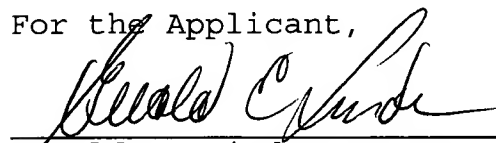
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION

(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

Charge any shortfall to Dep. Acct. 12-1445.

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (3) is being provided in addition to:

- (1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (4) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Copies of these references may be found in the file of commonly-owned, copending U.S. Patent Application No. 08/340,144 and, although NOT provided herewith, will be supplied upon request of the examiner.

It would appear that the most relevant ones of the references cited herein are those having the term "probe" or "test" in their title. For example, the following (from the list at pp. 3, et seq):

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TESTABLE RIBBON BONDING METHOD AND WEDGE BONDING TOOL FOR MICROCIRCUIT DEVICE FABRICATION		
<u>4,937,203</u>	<u>Eichelberger, et al.; 6/90</u>	<u>437/51</u>
METHOD AND CONFIGURATION FOR TESTING ELECTRONIC CIRCUITS AND INTEGRATED CIRCUIT CHIPS USING A REMOVABLE OUTER LAYER		
<u>4,884,122</u>	<u>Eichelberger, et al.; 11/89</u>	<u>357/71</u>
METHOD AND CONFIGURATION FOR TESTING ELECTRONIC CIRCUITS AND INTEGRATED CIRCUIT CHIPS USING A REMOVABLE OVERLAY LAYER		
<u>4,772,936</u>	<u>Reding, et al.; 9/88</u>	<u>357/80</u>
PRETESTABLE DOUBLE-SIDED TAB DESIGN		
<u>4,189,825</u>	<u>Robillard, et al.; 2/80</u>	<u>29/574</u>
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<u>5,432,677</u>	<u>Mowatt; 7/95</u>	<u>361/719</u>
MULTI-CHIP INTEGRATED CIRCUIT MODULE		
<u>5,414,299</u>	<u>Wang, et al.; 5/95</u>	<u>257/702</u>
SEMI-CONDUCTOR DEVICE INTERCONNECT PACKAGE ASSEMBLY FOR IMPROVED PACKAGE PERFORMANCE		
<u>5,397,245</u>	<u>Roebuck, et al.; 3/95</u>	<u>439/264</u>
NON-DESTRUCTIVE INTERCONNECT SYSTEM FOR SEMICONDUCTOR DEVICES		
<u>5,379,191</u>	<u>Carey, et al.; 1/95</u>	<u>361/777</u>
COMPACT ADAPTER PACKAGE PROVIDING PERIPHERAL TO AREA TRANSLATION FOR AN INTEGRATED CIRCUIT CHIP		
<u>5,359,493</u>	<u>Chiu; 10/94</u>	<u>361/719</u>
THREE DIMENSIONAL MULTI-CHIP MODULE WITH INTEGRAL HEAT SINK		
<u>5,350,947</u>	<u>Takekawa, et al.; 9/94</u>	<u>257/702</u>
FILM CARRIER SEMICONDUCTOR DEVICE		
<u>5,338,705</u>	<u>Harris, et al.; 8/94</u>	<u>437/217</u>
PRESSURE DIFFERENTIAL DOWNSET		
<u>5,327,327</u>	<u>Frew, et al.; 7/94</u>	<u>361/784</u>
THREE DIMENSIONAL ASSEMBLY OF INTEGRATED CIRCUIT CHIPS		
<u>5,321,277</u>	<u>Sparks, et al.; 6/94</u>	<u>257/48</u>
MULTI-CHIP MODULE TESTING		
<u>5,308,797</u>	<u>Kee; 5/94</u>	<u>437/209</u>
LEADS FOR SEMICONDUCTOR CHIP ASSEMBLY AND METHOD		
<u>5,306,670</u>	<u>Mowatt, et al.; 4/94</u>	<u>437/209</u>
MULTI-CHIP INTEGRATED CIRCUIT MODULE AND METHOD FOR FABRICATION THEREOF		
<u>5,289,346</u>	<u>Carey, et al.; 2/94</u>	<u>361/777</u>
PERIPHERAL TO AREA ADAPTER WITH PROTECTIVE BUMPER FOR INTEGRATED CIRCUIT CHIP		
<u>5,237,203</u>	<u>Massaron; 8/93</u>	<u>257/688</u>
MULTILAYER OVERLAY INTERCONNECT FOR HIGH-DENSITY PACKAGING OF CIRCUIT ELEMENTS		
<u>5,239,199</u>	<u>Chiu; 8/93</u>	<u>257/706</u>
VERTICAL LEAD-ON-CHIP PACKAGE		

<u>5,227,662</u>	<u>Ohno, et al.; 7/93</u>	<u>257/676</u>
COMPOSITE LEAD FRAME AND SEMICONDUCTOR DEVICE USING THE SAME		
<u>5,196,268</u>	<u>Fritz; 3/93</u>	<u>428/458</u>
INTEGRATED CIRCUIT INTERCONNECT LEADS RELEASABLY MOUNTED ON FILM		
<u>5,192,681</u>	<u>Chiu; 3/93</u>	<u>437/217</u>
LOW COST ERASABLE PROGRAMMABLE READ ONLY MEMORY PACKAGE		
<u>5,136,367</u>	<u>Chiu; 8/92</u>	<u>357/74</u>
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<u>5,127,570</u>	<u>Steitz, et al.; 7/92</u>	<u>228/103</u>
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<u>5,123,850</u>	<u>Elder, et al.; 6/92</u>	<u>439/67</u>
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<u>5,059,557</u>	<u>Cragon, et al.; 10/91</u>	<u>437/208</u>
METHOD OF ELECTRICALLY CONNECTING INTEGRATED CIRCUITS BY EDGE-INSERTION IN GROOVED SUPPORT MEMBERS		
<u>5,057,461</u>	<u>Fritz; 10/91</u>	<u>437/220</u>
METHOD OF MOUNTING INTEGRATED CIRCUIT INTERCONNECT LEADS RELEASABLY ON FILM		
<u>5,029,325</u>	<u>Higgins, III, et al.; 7/91</u>	<u>357/80</u>
TAB TAPE TRANSLATOR FOR USE WITH SEMICONDUCTOR DEVICES		
<u>5,025,306</u>	<u>Johnson, et al.; 6/91</u>	<u>357/75</u>
ASSEMBLY OF SEMICONDUCTOR CHIPS		
<u>5,024,746</u>	<u>Stierman, et al.; 6/91</u>	<u>204/297 W</u>
FIXTURE AND A METHOD FOR PLATING CONTACT BUMPS FOR INTEGRATED CIRCUITS		

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TESTABLE RIBBON BONDING METHOD AND WEDGE BONDING TOOL FOR MICROCIRCUIT DEVICE FABRICATION		
<u>5,127,570</u>	<u>Steitz, et al.; 3/95</u>	<u>228/103</u>
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<u>5,029,325</u>	<u>Higgins, III, et al.; 7/91</u>	<u>357/80</u>
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<u>4,982,264</u>	<u>Cragon, et al.; 1/91</u>	<u>357/75</u>
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<u>4,967,261</u>	<u>Niki, et al.; 10/90</u>	<u>357/70</u>
TAPE CARRIER FOR ASSEMBLING AN IC CHIP ON A SUBSTRATE		
<u>4,942,140</u>	<u>Ootsuki, et al.; 7/90</u>	<u>437/211</u>
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<u>4,937,203</u>	<u>Eichelberger, et al.; 6/90</u>	<u>437/51</u>
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<u>4,932,902</u>	<u>Crane, Jr.; 6/90</u>	<u>439/627</u>
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<u>4,931,149</u>	<u>Stierman, et al.; 6/90</u>	<u>204/15</u>
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<u>4,890,194</u>	<u>Derryberry; 12/89</u>	<u>361/386</u>
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<u>4,887,148</u>	<u>Mu; 12/89</u>	<u>357/74</u>
PIN GRID ARRAY PACKAGE SEMICONDUCTOR		
<u>4,884,122</u>	<u>Eichelberger, et al.; 11/89</u>	<u>357/71</u>
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<u>4,878,098</u>	<u>Saito, et al; 10/89</u>	<u>357/68</u>
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE		
<u>4,874,722</u>	<u>Bednarz, et al.; 10/89</u>	<u>437/209</u>
PROCESS OF PACKAGING A SEMICONDUCTOR DEVICE WITH REDUCED STRESS FORCES		
<u>4,874,721</u>	<u>Kimura, et al.; 10/89</u>	<u>437/209</u>
METHOD OF MANUFACTURING A MULTICHIP PACKAGE WITH INCREASED ADHESIVE STRENGTH		
<u>4,874,476</u>	<u>Stierman, et al.; 10/89</u>	<u>204/15</u>
FIXTURE FOR PLATING TALL CONTACT BUMPS ON INTEGRATED CIRCUIT		
<u>4,861,452</u>	<u>Stierman, et al.; 8/89</u>	<u>204/297 W</u>
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<u>4,855,867</u>	<u>Gadzik; 8/89</u>	<u>361/306</u>
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<u>4,796,078</u>	<u>Phelps, Jr., et al; 2/89</u>	<u>357/68</u>
PERIPHERAL/AREA WIRE BONDING TECHNIQUE		
<u>4,772,936</u>	<u>Reding, et al.; 9/88</u>	<u>357/80</u>
PRETESTABLE DOUBLE-SIDED TAB DESIGN		
<u>4,764,804</u>	<u>Sahara, et al.; 8/88</u>	<u>357/81</u>
SEMICONDUCTOR DEVICE AND PROCESS FOR PRODUCING THE SAME		
<u>4,751,482</u>	<u>Fukuta, et al.; 6/88</u>	<u>333/247</u>
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING A MULTI-LAYERED WIRING BOARD FOR ULTRA HIGH SPEED CONNECTION		
<u>4,750,089</u>	<u>Derryberry, et al.; 6/88</u>	<u>361/388</u>
CIRCUIT BOARD WITH A CHIP CARRIER AND MOUNTING STRUCTURE CONNECTED TO THE CHIP CARRIER		
<u>4,721,993</u>	<u>Walter; 1/88</u>	<u>357/70</u>
INTERCONNECTION TAPE FOR USE IN TAPE AUTOMATED BONDING		
<u>4,710,798</u>	<u>Marcantonio; 12/87</u>	<u>357/80</u>
INTEGRATED CIRCUIT CHIP PACKAGE		
<u>4,709,468</u>	<u>Wilson; 12/87</u>	<u>437/209</u>
METHOD FOR PRODUCING AN INTEGRATED CIRCUIT PRODUCT HAVING A POLYIMIDE FILM INTERCONNECTION STRUCTURE		
<u>4,695,872</u>	<u>Chatterjee; 9/87</u>	<u>357/75</u>
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<u>4,685,998</u>	<u>Quinn, et al.; 8/87</u>	<u>156/633</u>
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FLEXIBLE FILM SEMICONDUCTOR CHIP CARRIER		
<u>4,670,770</u>	<u>Tai; 6/87</u>	<u>357/60</u>
INTEGRATED CIRCUIT CHIP-AND-SUBSTRATE ASSEMBLY		
<u>4,649,415</u>	<u>Herbert; 3/87</u>	<u>357/74</u>
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<u>4,628,406</u>	<u>Smith, et al.; 12/86</u>	<u>361/386</u>
METHOD OF PACKAGING INTEGRATED CIRCUIT CHIPS, AND INTEGRATED CIRCUIT PACKAGE		
<u>4,627,151</u>	<u>Mulholland, et al.; 12/86</u>	<u>29/569 R</u>
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ELECTRONIC CIRCUIT INTERCONNECTION SYSTEM		
<u>4,514,750</u>	<u>Adams; 4/85</u>	<u>357/70</u>
INTEGRATED CIRCUIT PACKAGE HAVING INTERCONNECTED LEADS ADJACENT THE PACKAGE ENDS		
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<u>4,410,905</u>	<u>Grabbe; 10/83</u>	<u>357/80</u>
POWER, GROUND AND DECOUPLING STRUCTURE FOR CHIP CARRIERS		
<u>4,385,202</u>	<u>Spinelli, et al.; 5/83</u>	<u>174/68.5</u>
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ELECTRONICS CIRCUIT DEVICE AND METHOD OF MAKING THE SAME		
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INTEGRATED TEST AND ASSEMBLY DEVICE		

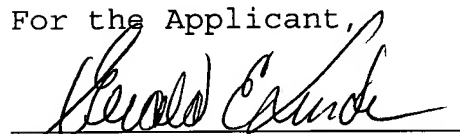
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<u>3,772,575</u>	<u>Hegarty, et al.; 11/73</u>	<u>317/235 R</u>
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<u>3,689,991</u>	<u>Aird; 9/72</u>	<u>20/577</u>
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<u>3,611,061</u>	<u>Segerson; 10/71</u>	<u>317/234 R</u>
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<u>3,390,308</u>	<u>Marley; 3/66</u>	<u>317/100</u>
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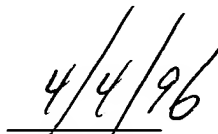
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SEMICONDUCTOR CONNECTION COMPONENTS AND METHODS WITH
RELEASABLE LEAD SUPPORT

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Attorney Docket No. 95-553-US

I hereby certify that this paper is being deposited as first class mail with the United States Postal Service in an envelope with sufficient postage addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231, on April 4, 1996

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Title of the Invention:

PROBE CARD ASSEMBLY AND KIT, AND METHODS OF USING SAME

Inventors: ELDRIDGE, et al.

Filing Date: 11/9/95

Serial Number: 08/554,902

SUPPLEMENTAL INFORMATION DISCLOSURE CITATION

(Substitute PTO-1449)

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION is being submitted **prior to an action on the merits.**

NO FEE IS REQUIRED.

Charge any shortfall to Dep. Acct. 12-1445.

This SUPPLEMENTAL INFORMATION DISCLOSURE CITATION (4) is being provided in addition to:

- (1) INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (2) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96
- (3) SUPPLEMENTAL INFORMATION DISCLOSURE CITATION, filed 4/4/96

Although not required, TITLES for the patent references are provided herewith, as an aid to the examiner.

Generally, the references presented herein are arranged in groups, as follows:

GROUP 1. References related to solder balls or solder pads as terminals of a semiconductor package or chip carrier. These references have particular pertinence to this application (08/584,981), and may be found in the file thereof.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, but will be provided upon request.

GROUP 2. References related to probing and/or testing semiconductor devices. These references have particular pertinence to this application and to commonly-owned, copending U. S. Patent Application No. 08/558,332.

COPIES OF THESE REFERENCES ARE ENCLOSED HEREWITH.

GROUP 3. References related to previously-cited patent references and miscellaneous references of interest.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

GROUP 4. References cited in PCT/US94/13373

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

GROUP 5 References dealing with making connections to electronic components.

COPIES OF THESE REFERENCES ARE **NOT** ENCLOSED HEREWITH, AND MAY BE FOUND IN THE FILE OF commonly-owned, copending U.S. Patent Application No. 08/340,144. Copies of these references will be provided upon request.

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